

--Summary of the Invention: --.

Page 2, replace the paragraph beginning on line 7 with:

--This object is achieved by a synchronous integrated memory having a control unit for producing a first internal clock, which leads the external clock by a specific phase shift, an output circuit, which can be activated via an activation input, which, in the activated state, starts an output process for the data to be read out, in synchronism with the first internal clock, and which outputs the data with the specific phase shift with respect to the first internal clock, that is to say in synchronism with the external clock, at the data connection, a clock generator for a second internal clock, which is synchronized to the external clock, a counting unit, which starts a counting process for recording the number of successively following first levels of the first internal clock as soon as the second internal clock for the first time assumes a first level while an output control signal is at a first level, and which activates the output circuit via its activation input as soon as the number of successively following first levels of the first internal clock has reached a predetermined value. Advantageous refinements and developments of the invention are the subject matter of the dependent claims.--

Page 5, between lines 18 and 20, insert:

--Brief Description of the Drawings:--.

Page 6, between lines 3 and 5, insert:

--Description of the Preferred Embodiment:--.

Replace the paragraph bridging pages 11 and 12 with:

--Thus, as soon as the output control signal PAR assumes a positive level and provided the second internal clock CLKI2 is at a low level, the counting unit CT from Figure 1 thus counts the subsequent positive levels of the first internal clock CLKI1. In this case, the output signal of the counting unit CT is synchronized to the first internal clock CLKI1, since the register elements RE are clocked by it.--

Page 13, top, change "Patent claims" to -- We Claim: --.

In the Claims:

Cancel claims 1-5 and enter the following new claims:

--6. A synchronous integrated memory for holding data and to be connected to an external clock producing an external clock signal, the memory comprising:

a data connection;

an output control connection carrying an output control signal having output levels including a given level;

a control unit outputting a first internal clock signal to lead an external clock signal by a given phase shift, said first internal clock signal having first signal levels including said given level;

a clock generator generating a second internal clock signal synchronized to the external clock signal and having second levels including said given level;

a counting unit having an activation connection carrying an activation signal defining an activated state;

said counting unit starting a counting process for recording a number of successively following given levels of said first internal clock signal as soon as said second internal clock signal for a first time assumes said given level while said output control signal is at said given level,

an output circuit connected to said activation connection, said activated state starting an output process for reading data out of the memory in synchronism with said first internal clock signal;

said output circuit outputting the data at said data connection with said given phase shift with respect to said first internal clock signal and in synchronism with the external clock signal; and

said counting unit activating said output circuit through said activation connection as soon as said number of successively following given levels of said first internal clock signal has reached a predetermined value.

7. The memory according to claim 6, including a variable control signal connection carrying a variable control signal for setting said predetermined value of said number of successively following given levels of said first internal clock signal, said variable control signal connection connected to said counting unit for supplying said variable control signal to said counting unit.

8. The memory according to claim 7, wherein:

said counting unit has a shift register with a series circuit of register elements;

each of said register elements has at least two inputs and at least one output;

one of said at least two inputs of a first of said register elements is connected to said output control connection for supplying said first register element with said output control signal at said one input;

another of said at least two inputs of said first register element is connected to said clock generator for clocking said first register element with said second internal clock signal at said another input;

others of said register elements are clocked as a function of said first internal clock signal;

a multiplexer has a switching state, inputs, and an output;

said inputs of said multiplexer are connected to said at least one output of some of said register elements;

said output of said multiplexer is connected to said activation connection for connecting said at least one output of at least one of said register elements to said activation connection; and

said switching state of said multiplexer is set by said variable control signal.

9. The memory according to claim 6, wherein said clock generator has a delay element and produces said second internal clock signal from said first internal clock signal with said delay element.

10. The memory according to claim 9, wherein said control unit has:

a variable delay unit with a variable delay unit input, a variable delay unit output, and a variable delay unit control input;

a control unit input connected to the external clock;

a control unit output connected to said control unit input through said variable delay unit, said control unit output outputting said first internal clock signal;

a phase comparator with:

a first comparator input connected to said control unit input;

a second comparator input connected to said control unit output through said delay element of said clock generator; and

a comparator output connected to said variable delay unit control input.--

In the Drawings:

Please approve the corrections to Fig. 1 marked in red on the attached new Fig. 1.

In the Abstract:

Please replace the Abstract of the Disclosure with the new Abstract of the Disclosure, attached hereto as a separate sheet.

Remarks:

The preliminary amendment is being filed in an effort to present an application in proper U.S. format and to present claims in proper U.S. claim idiom for examination.

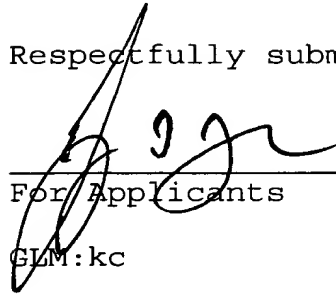
The newly entered claims are fully supported in the original claims.

New Fig. 1 of the drawings is submitted for approval.

Specifically, functional blocks in Fig. 1 have been given labels.

An early action on the merits of the claims is requested.

Respectfully submitted,



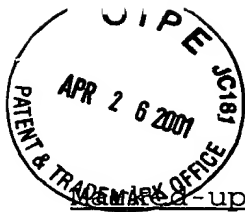
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Advantageous refinements and developments of the invention are the subject matter of the dependent claims.--.

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--Thus, as soon as the output control signal PAR assumes a positive level and provided the second internal clock CLKI2 is at a low level, the counting unit CT from Figure 1 thus counts the subsequent [positieve] positive levels of the first internal clock CLKI1. In this case, the output signal of the counting unit CT is synchronized to the first internal clock CLKI1, since the register elements RE are clocked by it.--.